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	FILING DATE June 19, 2003	GROUP ART UNIT 2811

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
CK	1.	Chatterjee et al., "CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator," IEEE, IEDM, 0-7803-4774-9/98, pp. 777-780 (1998)
CK	2.	Chen et al., "0.18μm Metal Gate Fully-Depleted SOI MOSFETs for Advanced CMOS Applications," Symposium on VLSI Technology Digest of Technical Papers, pp. 25-26 (1999)
CK	3.	Ducroquet et al., "Full CMP Integration of CVD TiN Damascene Sub-0.1-μm Metal Gate Devices For ULSI Applications," IEEE Transactions on Eectron Devices, Vol 48, No. 8, pp. 1816-1821 (2001)
CK	4.	Ferguson et al., "Titanium Nitride Metal Gate Electrode: Effect of Nitrogen Incorporation," Advanced Metallization Conference 2001 (AMC 2001), pp. 115-119
CK	5.	Hobbs et al., "Sub-Quarter Micron CMOS Process for TiN-Gate MOSFETs with TiO2 Gate Dielectric formed by Titanium Oxidation," Advanced Products Research and Development Lab, Symposium on VLSi Technology Digest of Technical Papers, pp. 133-134 (1999)
CK	6.	Maiti et al., "PVD TiN Metal Gate MOSFETs on Bulk Silicon and Fully Depleted Silicon-On-Insulator (FDSOI) Substrates for Deep Sub-Quarter Micron CMOS Technology," IEEE, IEDM, 0-7803-4774-9/98, pp. 781-784 (1998)
CK	7.	Park et al., "Robust Ternary Metal Gate Electrodes for Dual Gate CMOS Devices," IEEE, IEDM, 0-7803-7050-3/02, pp. 671-674 (2001)
CK	8.	Polishchuk, "Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion," IEEE Electron Device Letter, Vol. 22, No. 9 pp, 444-446 (2001)
CK	9.	Wakabayashi et al., "A Novel W/TiNx Metal Gate CMOS Technology using Nitrogren-Concentration-Controlling TiNx Film," IEEE, IEDM, 0-7803-5410-9/99, pp. 253-256 (1999)
CK	10.	Yagishita et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 μm Regime," IEEE Transactions on Electron Devices, Vol. 47, No. 5, pp. 1028-1034 (2000)
CK	11.	Yagishita et al., "Reduction of Threshold Voltage Deviation in Damascene Metal Gate MOSFETs," IEEE, IEDM, 0-7083-5410-9/99, pp. 257-260 (1999)
CK	12.	Yeo et al., "Dual-Metal Gate CMOS Technology with Ultrathin Silicon Nitride Gate Dielectric," IEEE Electronic Device Letters, Vol. 22, No. 5, pp. 227-229 (2001)
CK	13.	Zhong et al., "Electrical Properties of RuO_2 Gate Electrodes for Dual Metal Gate Si-CMOS," IEEE Electron Device Letters, Vol. 21, No. 12, December 2000, pp. 593-595

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EXAMINER Christy Haracek	DATE CONSIDERED 7/29/04

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